	Subclass	CLASSIFICATION
796/60 796/60 796/60	Class	ISSUE CLA



PATENT NUMBER

50906

U.S. UTILITY Patent Appl	ication	_	
RE O.I.P.E. SCANNED KG 2 G.A.	PATENT DATE	·	 ,

Fariborz Assaderaghi Harold Chase Stephen Runyon Method for producing an integrated circuit capacitor	APPLICATION NO. 09/964127	CONT/PRIOR D	CLASS	SUBCLASS 394	ARTUNIT Z822	EXAMINER	. ;
Method for producing an integrated circuit capacitor	Harold Cha	se	i ,			Ü	
1	! Method for	producir	ng an inte	egrated c	ircuit capa	acitor	.•

ISSUING CLASSIFICATION							
ORIGI	IAL	1.7	CROSS REFERENCE(S)				
CLASS	SUBCLAS	S CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
INTERNATION	L CLASSIFICAT	ION					
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TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent		I		NOTICE OF ALLOWANCE MAILED	
subsequent to (date)					
has been disclaimed.	(Assistant Examiner)		(Date)	•	
The term of this patent shall		•			,
not extend beyond the expiration date of U.S Patent. No			ISSUE FEE		
·		, •		Amount Due	Date Paid
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☐ The terminalmonths of	ISSUE		ISSUE BAT	E BATCH NUMBER	
this patent have been disclaimed.	(Legal Instruments Examiner) (Date)		(Date)		
WARNING: The information disclosed herein may be resident a Tradem					i, Sections 122, 181 and 36
om PTO-438A Rev. 6/99)	·		FILED WITH:	DISK (CRF)	FICHE CD-RO